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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,019	06/08/2001	Seiichi Mori	209665US-2	7457

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EXAMINER
PHAM, HOAI V

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/876,019	MORI, SEIICHI	
	Examiner	Art Unit	
	Hoai V Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *7-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restriction

1. Applicant's election with traverse of claims 1-6 in Paper No. 10 is acknowledged. The traversal is on the ground(s) that "The criteria are (1) the inventions must be independent or distinct as claimed and (2) there must be a serious burden on the examiner if restriction is not required. Regarding the second criterion, if the search and examination of an entire application can be made without serious burden, the Examiner must examine on the merits, even though it includes claims too distinct or independent invention". This is not found persuasive because

a) The above two different classifications show the need for two entirely different fields of a search.

b) The inventions are in different statutory classes which have different case law basis for examination.

c) Non-restriction would mean that if one of the inventions were held to be unpatentable then the other would also be inherently held to be unpatentable.

Therefore, restriction is proper since there are apparently two different inventive concepts in making the device and in the device itself.

The requirement is still deemed proper and is therefore made FINAL.

Information Disclosure Statement

2. The related pending application 09/876,019; 09/956,986; 09/984,590; 10/098,130 and 10/214,582 have been considered.

Drawings

3. Figures 35-36 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 3-5 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 3, the phrase "different n-type impurities are doped into said floating gates of said nonvolatile memory cells and gate electrodes of NMOS transistors in said peripheral circuit, and a p-type impurity is doped into said gate electrodes of PMOS

transistors in said peripheral circuit" is not supported in the specification since the specification shows the impurities are doped **in the substrate** to form source and drain regions (page 17, lines 32-35).

Claims 4-5, the phrase "phosphorus is doped into said floating gates of said nonvolatile memory cells, and arsenic is doped into said gate electrodes of NMOS transistors in said peripheral circuit" is not supported in the specification since the specification shows the impurities are doped **in the substrate** to form source and drain regions (page 17, lines 32-35).

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-6, lines 14-16, the phrase "then being maintained in self alignment with said device isolation insulating film" renders the claim indefinite. It is not clear which layer is in self-alignment with said device isolation insulating film.

Claim 1, lines 16-17, the phrase "and impurities being doped thereto under different conditions from each other" renders the claim indefinite. It is not clear where the impurities located. Does <u>different conditions</u> mean different doping impurities types i.e. type of ions used? or does <u>different conditions</u> mean energy used to diffuse the concentration of the doping impurities?

Claim 2, lines 2-3, the phrase "wherein said transistors in said peripheral circuit have at least two gate insulating films different in thickness" renders the claim indefinite. Does the transistor have two gate insulating films different in thickness? Or does the first transistor have a gate insulating film different from that of the second transistor?

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

10. Claims 1 and 6, as best understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Shimizu et al. [U.S. Pat. 6,342,715].

Shimizu et al. (figs. 13A-13B, cols. 18-19) a semiconductor memory integrated circuit comprising:

a semiconductor substrate (1);

a device isolation insulating film (2) buried in grooves formed into said semiconductor substrate;

a cell array (31)having an arrangement of electrically erasable and programmable nonvolatile memory cells made by stacking

floating gates (5) and control gates (7) on said semiconductor substrate; and

a peripheral circuit (32) disposed around said cell array on said semiconductor substrate, wherein at least bottom layer (5L) of said floating gates and the bottom layer (35L) of gate are in self alignment with said device isolation insulating film (2) and wherein the impurities regions (9 and 39) formed in the substrate on both sides of the floating gate and the transistor.

Note that process limitation (at least the bottom layer of said floating gates of said nonvolatile memory cells and at least the bottom layer of gate electrodes of transistors in said peripheral circuit being formed **before** said device isolation insulating film is buried.) do not carry weight in a claim drawn to structure. *In re Thorpe*, 227 USPQ 964 (Fed. Cir. 1985). In addition, a "product by process" limitation is directed to the product per se, no matter how actually made, in re Hirao, 190 USPQ 15 and 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90; and *In re Marosi et al.*, 218 USPQ 289; all of which made clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product by a new method is not patentable as a product, whether claimed in "product by process" claims or not.

With respect to claim 6, Shimizu et al. discloses that the floating gates of the nonvolatile memory cells comprise of a first-layer (5L) gate electrode material film in self alignment with the device isolation insulating film (2) and a second-layer (5U) gate

electrode material film stacked on the first gate electrode material film, the control gates comprise of a third-layer (7) electrode material film, and the gate electrodes in said peripheral circuit have a three-layered structure including said first- to third-layer (35L, 35U, 37) gate electrode material films (fig. 13B).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2-5, as best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. [U.S. Pat. 6,342,715] in view of Takebuchi [U.S. Pat. 6,417,051].

With respect to claim 2, Shimizu et al. does not disclose that a first transistor having the gate insulating film is different in thickness from a second transistor in the peripheral circuit. However, Takebuchi discloses that the first transistor having the gate insulating film (64) is different in thickness from the gate insulating film (67) of second transistor in the peripheral circuit to form a high and low voltage transistors (fig. 9, col. 19, lines 19-23). Therefore, it would have been obvious to the skilled in the art to use the first transistor having the gate insulating film of a different thickness from the gate insulating film of the second transistor into the device of Shimizu et al. in order to form a

high and low voltage transistors that can be readily used in the peripheral circuit and logic device.

With respect to claims 3-5, Shimizu et al. does not mention that in the peripheral circuit having a n-type impurity is doped into the NMOS transistor to form source/drain regions and a p-type impurity is doped into the PMOS transistors to form source/drain regions. However, Takebuchi discloses that in the peripheral circuit having a n-type impurity is doped into the NMOS transistor to form source/drain regions (87) and a p-type impurity is doped into the PMOS transistors to form source/drain regions (83) (Fig. 9, col. 19, lines 35-48). Therefore, it would have been obvious to the skilled in the art to have the n-type impurity is doped into the NMOS transistor to form source/drain regions and the p-type impurity is doped into the PMOS transistors to form source/drain regions into the device of Shimizu et al. for forming a CMOS that can be readily used in the peripheral circuit.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai V Pham whose telephone number is 703-308-6173. The examiner can normally be reached on 6:30A.M. - 6:00P.M..

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

15. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HP
Hoai Pham
November 26, 2002

Wael Fahmy

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800